# Microcomputer design — 4

## Practical realisation of a microcomputer system

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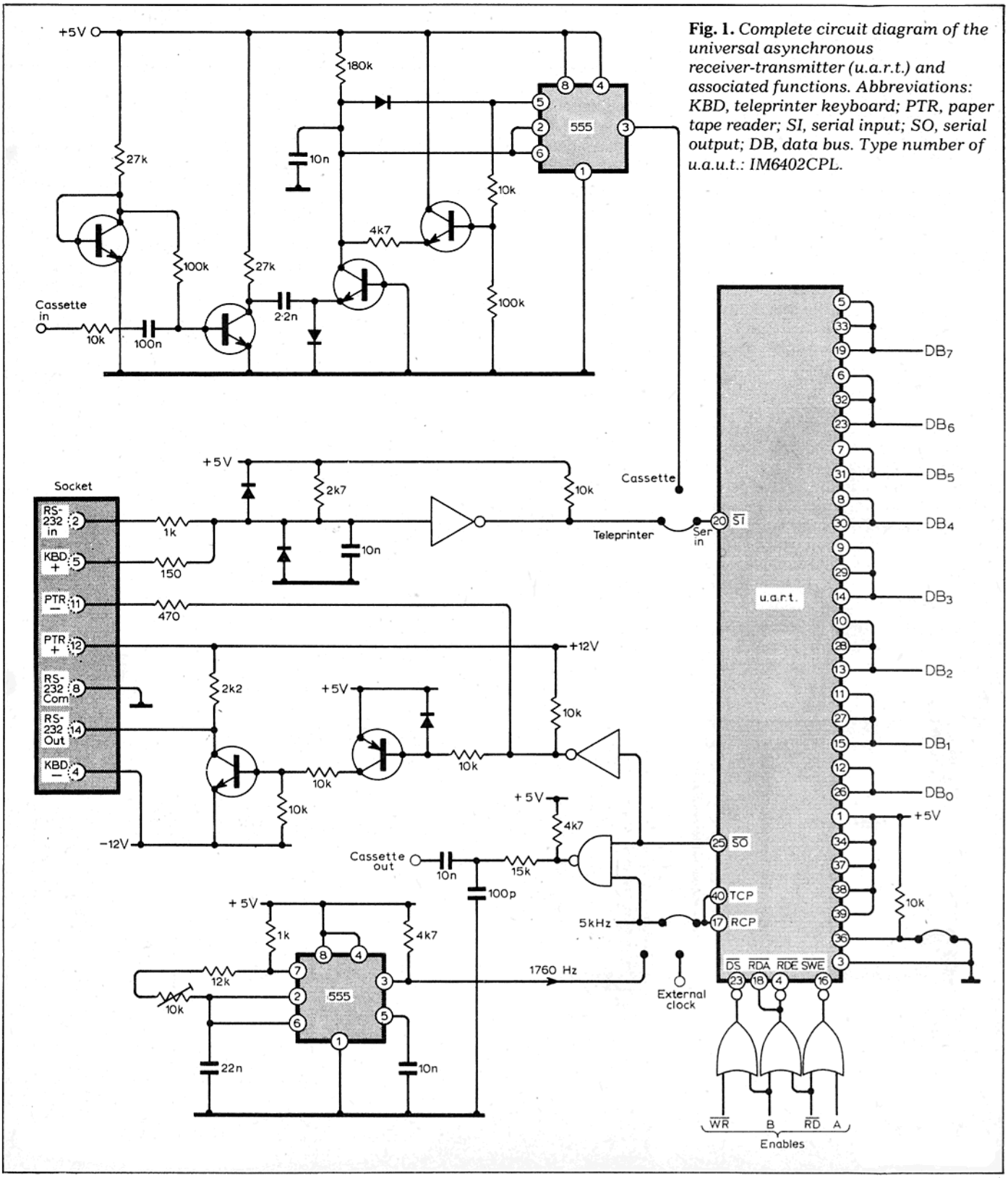


**Fig. 1.** *Complete circuit diagram of the universal asynchronous receiver-transmitter (u.a.r.t.) and associated functions. Abbreviations: KBD, teleprinter keyboard; PTR, paper tape reader; SI, serial input; SO, serial output; DB, data bus. Type number of u.a.u.t.: IM6402CPL.*

THIS MONTH the description of those peripherals of the microcomputer system outlined in the January issue is completed by a circuit diagram of the universal asynchronous receiver-transmitter (u.a.r.t.). As explained last month, the purpose of the u.a.r.t. is to provide a transformation between the 8-bit parallel data within the computing system and the type of serial digital information which can be handled by peripheral devices such as the audio cassette recorder. The u.a.r.t. is shown in Fig. 1, and it will be seen that this has connections to the 8-bit data bus of the computer system on the right (labelled $DB_0$ to $DB_7$) and connections for the serial input and output information on the left (labelled SI and SO, negated).

## Clock arrangements

As also mentioned last month, the rate at which the data is shifted into and out of the u.a.r.t. is determined by a clock pulse signal applied to the receiver and transmitter clock connections on the u.a.r.t. (pin 17, labelled RCP, and pin 40, labelled TCP). There are in fact three clock pulse generators available to the system. The first of these is provided elsewhere in the computer by a crystal oscillator and divider chain, which produces a 5kHz clock signal, and this is fed to the u.a.r.t. by a link as shown at the bottom of the diagram. The second clock generator is a circuit at the bottom left of Fig. 1. This is a simple oscillator based on a 555 i.c. which can be adjusted to operate at 1760Hz, and as shown this signal can be fed to pins 17 and 40 on the u.a.r.t. by means of the link. The third clock generator is any external source the user may care to apply, and this again is fed into pins 17 and 40 on the u.a.r.t. by the link as shown at the bottom right.

As already mentioned, since a stop bit and a start bit are added to the byte, there are 10 bits in each word transmitted. This, however, can be increased to 11 bits by adding another stop bit, which can be done by applying +5V to pin 36 on the u.a.r.t. by means of the 10kΩ resistor and removable link.

Serial digital information is recorded on the audio cassette recorder in the form of a modulated tone. This tone is provided by the 5kHz clock signal shown in Fig. 1, which is modulated by gating it with the serial data emerging from $\overline{SO}$ on the u.a.r.t. The resulting modulated 5kHz signal goes to the "cassette out" terminal. The playback signal from the cassette recorder (applied to the terminal "cassette in") is therefore a series of bursts of 5kHz tone corresponding to the serial data stream. To convert these tone bursts back to conventional logic levels there is a tone detector circuit. This is shown at the top of Fig. 1, and is made up from a 555 i.c. and associated components.

The serial input to the u.a.r.t. is connected by a link to whichever source is chosen by the user.

## Peripheral 4—visual display

In any computer system of this type it is required that the user be presented with data from the machine. For programme development this may mean the presentation of several hundred characters. At the same time the cost of displaying alphanumeric characters should be minimised. The method chosen for this project is a "memory plane peripheral" and is not sited on ports as conventional i/o but consists of logic which shares a section of the memory. This logic is designed to present a composite video signal to a domestic television receiver in such a way that the contents of this memory section are interpreted as characters. Any possible conflict of access to the memory between the processor and the logic has been resolved by giving the processor absolute priority. As a concession to appearance the video signal is blanked during c.p.u. access. It is as though a section of memory is exactly mapped on to a visible plane.

*(To be continued)*

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one alumina substrate. Anodised aluminium capacitors ranging from 2 to 400pF, and nichrome resistors ranging from 4 to 200Ω, are used.

## Acknowledgements

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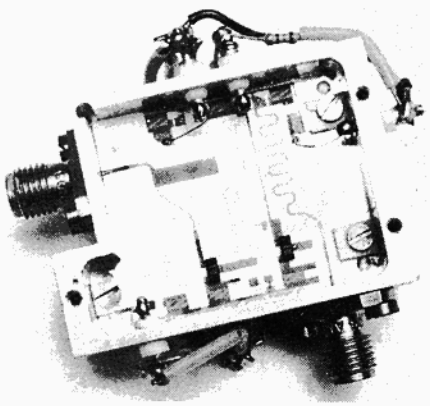

**Fig. 10.** *A 900MHz transistor amplifer.*

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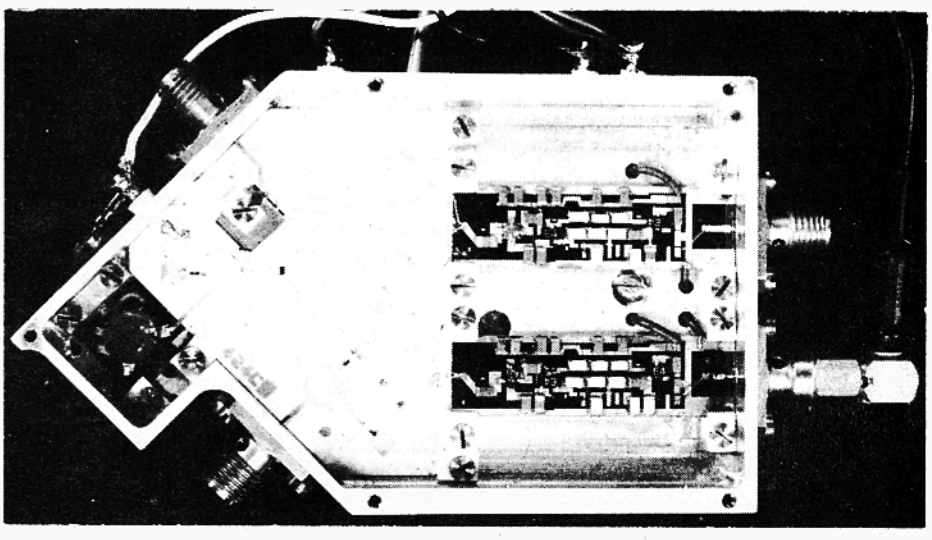

**Fig. 9.** *An integrated X-band Doppler receiver.*